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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/728,449

12/05/2003

William Planey

LOVE-51.CON

9343

7590

01/23/2006

WAGNER, MURABITO HAO LLP

Third Floor

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San Jose, CA 95113

EXAMINER

NGUYEN, DAO H

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/728,449

Applicant(s)

PLANEY, WILLIAM

Examiner

Dao H. Nguyen

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 November 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 November 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

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DETAILED ACTION

1. In response to the communications dated 11/01/2005, claims 1-10 are active in this Application.

Claims 11-22 have been cancelled.

Terminal Disclaimer filed 11/01/2005 have been considered and approved.

Correction to the drawing have been considered and accepted.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements is/are:

the angular extensions formed with the X-lead frame to make physical and electrical contact with the upper surface of the die, as discussed on page 7, lines 16-19 of the specification; and

a source pad having a configuration being designed to make mechanical and electrical contact with a source region located on the lower surface of the die as discussed on page 8, lines 6-9 of the specification.

These elements are essential because without them, the die would not be hold in place.

4. Claim(s) 1-10 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention (See MPEP § 2172.01).

Claim 1 states that the semiconductor die is disposed between the mounting surface and the X-lead frame without bonding to the mounting surface and without bonding to the semiconductor die. This is not clearly defined and distinctly pointed out the subject matter which is claimed as the Applicant's invention, because it is not clearly defined that without bonding to either the mounting surface or X-lead frame, how the die would be hold to its position? How it would be disposed between the mounting surface and the X-lead frame?

According to the specification, page 7, lines 16-19, the X-lead frame is formed with angular extensions that are in physical contact with the upper surface of the die. The angular extensions hold the die in place as well as make electrical contact with the drain of the die. Also, page 8, lines 6-9 of the specification discuss that the underlying support structure, or the mounting surface, includes a source pad. The configuration of the source pad is designed to make mechanical and electrical contact with a source region on the lower surface of the die. Thus, it is clearly that both the X-lead frame and the mounting surface are in both physical/mechanical as well as **electrical contacts, or**

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bonds, to the die. Essentially, such contact(s) or bond(s) is/are made via the angular extensions and the source pad and source region.

Note that according to Merriam-Webster's Collegiate Dictionary, tenth edition, bond or bonding means that an adhesive, cementing material, or fusible ingredient that combines, unites, or strengthens. Bond or bonding also means that something that binds or restrains (to bind means to make secure by tying, to fasten together, to exert a restraining effect); a uniting or binding element or force; to bond is to provide a bond for or cause to provide such a bond; to hold together or solidify by or as if by means of a bond or binder.

Claims 2-10 depend from rejected claim 1 and include all of the limitations of claim 1 thereby rendering these dependent claims indefinite.

Claim Rejections - 35 U.S.C. § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 1 and 7 - 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dunaway et al., EU Patent Application Publication No. 370745 in view of the

Admitted Prior Art (Admission).

Regarding claim 1, Dunaway disclose a system mounting a semiconductor die within the package comprising:

- a mounting surface 22;
- a lead frame 10 coupled to the mounting surface 22, and
- said semiconductor die 42, wherein the die 42 is disposed between the mounting surface and the lead frame.

Dunaway does not teach that the lead frame is an X-lead frame.

However, figure 4 of Admission illustrates an X-lead frame with four angular tabs 430.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to replace lead frame 10 of Dunaway with the X-lead frame of the Admission, in order to provide conductive elements for use in interconnecting the lead frame with one of the other electronic device (it is noticed that in col. 5, lines 5 - 10, Dunaway et al. teach that "it is appreciated that lead-frames are variously constructed and shaped").

Regarding claims 7 - 10, Dunaway in view of Admission disclose all claimed limitations, except for the package and the terminals being conformed to an S08 configuration.

However, it is known that in order to be adapted by majority of the semiconductor industries, the package has to conform to the S08 configuration. So, it is inherent that the package structure in Dunaway is conformed to an S08 configuration in order to be adapted by the semiconductor industries.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dunaway et al. (EU Patent Application Publication No. 370745) in view of the Admitted Prior Art (Admission) and further in view of Tsivdis, U.S. Patent No. 5,293,058.

Regarding claim 2, Dunaway in view of Admission disclose all claimed limitations, except for the JFET having a surface region defining a source, a surface region defining a drain and a surface region defining a gate.

It is well known, and also taught by Tsivdis that MOSFET or JFET have a surface region 24 (fig. 4 of Tsivdis) defining a source, a surface region 22 defining a drain and a surface region 13 and 14 defining a gate.

Therefore, it is inherent that the transistor in Dunaway et al. having a surface region defining a source, a surface region defining a drain and a surface region defining a gate.

8. Claim(s) 1-10 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,040,626 To Cheah et al., in view of Yu et al., U.S. Patent No. 6,809,408.

Regarding claim 1, Cheah discloses a system mounting a semiconductor die 16 within a package 22, as shown in figs. 1-9, comprising:

a mounting surface 12/13;
a lead frame 30/34 coupled to said mounting surface 12/13, and
said semiconductor die 16, wherein said semiconductor die 16 is disposed between said mounting surface 12/13 and said lead frame.

Cheah does not teach that the lead frame is an X-lead frame.

Yu discloses a semiconductor package comprising a lead frame having an X-shaped or an X-lead frame. See fig. 3.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the lead frame of Cheah to have an X-shaped as that of Yu in order to reduce the contact area between the die and the lead frame, thereby significantly diminish the thermal stress applied from the lead frame to the die. See col. 5, lines 51-59 of Yu.

Regarding claim 2, Cheah/Yu disclose the package wherein said semiconductor die is a semiconductor power MOSFET, which definitely could be a JFET, having a surface region defining a source, a surface region defining a drain and a surface region defining gate. See col. 2, lines 47-64; col. 3, lines 31-47.

Regarding claim 3, Cheah/Yu disclose the power semiconductor package wherein electrical coupling between said drain 18 and said X-lead frame is realized by angular projections of said X-lead frame contacting said drain 18. See figs. 3-9 of Cheah. Note that in a CMOS, source and drain regions can be technically interchangeable or switchable.

Regarding claim 4, Cheah/Yu disclose the power semiconductor package wherein said X-lead frame is bonded to a first terminal 12B disposed on said mounting surface. See figs. 3-9, and col. 5, lines 17-29 of Cheah.

Regarding claim 5, Cheah/Yu disclose the power semiconductor package wherein a second terminal 12a disposed on said mounting surface is electrically connected to said source. See fig. 3-9 of Cheah.

Regarding claim 6, Cheah/Yu disclose the power semiconductor package wherein a third terminal 12c disposed on said mounting surface is electrically connected to said gate 19. See fig. 5 of Cheah.

Regarding claim 7, Cheah/Yu disclose the semiconductor package wherein said package is sized and shaped to conform to an S08 configuration. See col. 1, lines 12-19; col. 3, lines 64-67 of Cheah.

Regarding claim 8, Cheah/Yu discloses the semiconductor package wherein said first terminal is a solid terminal spanning the full width of four leads and the spaces between four leads on one side of said S08 package. See figs. 3-9 of Cheah, and fig.3D of Yu.

Regarding claim 9, Cheah/Yu disclose the semiconductor package wherein said second terminal is a solid terminal spanning a width of three leads and the spaces between three leads on a side of said S08 package opposite to said first terminal. See figs. 3-9 of Cheah, and fig. 3D of Yu.

Regarding claim 10, Cheah/Yu disclose the semiconductor package wherein said third terminal is a solid terminal spanning a width of a single lead on a side of said S08 package opposite to said first terminal. See fig. 3-9 of Cheah.

Conclusion

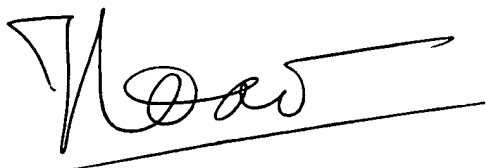
9. **THIS ACTION IS MADE FINAL.** A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date

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the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday 9:00am - 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached on (571)272-1787. The fax numbers for all communication(s) is (571)273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.



Dao H. Nguyen
Art Unit 2818
January 9, 2006



David Nelms
Supervisory Patent Examiner
Technology Center 2800

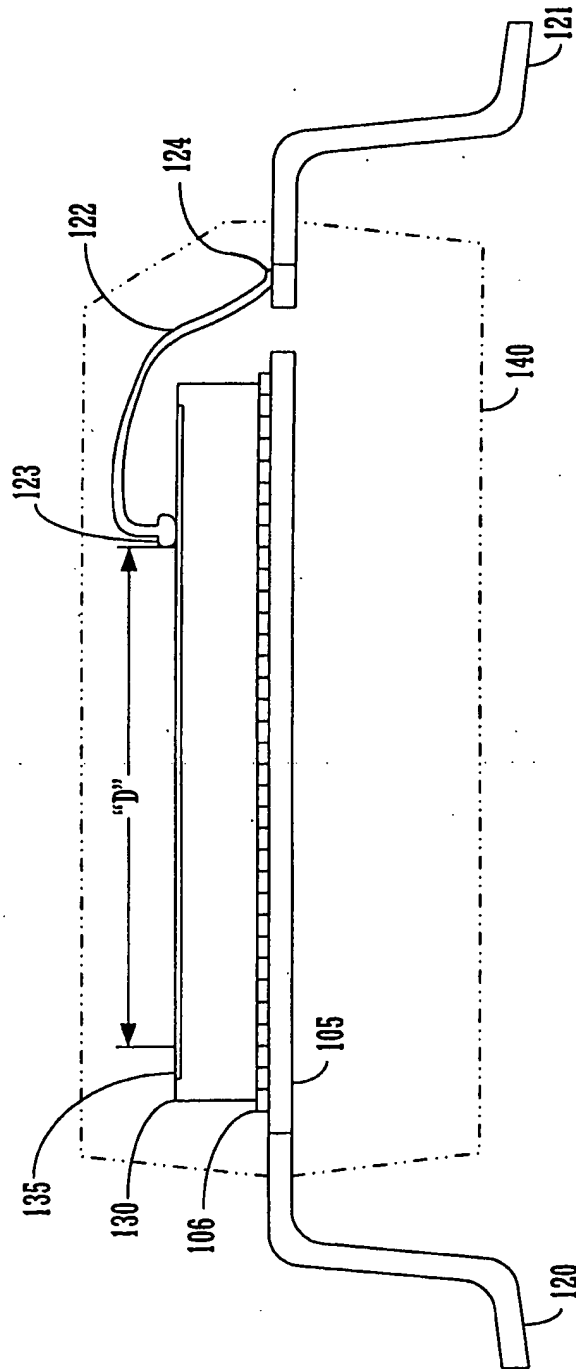


Replacement Sheet

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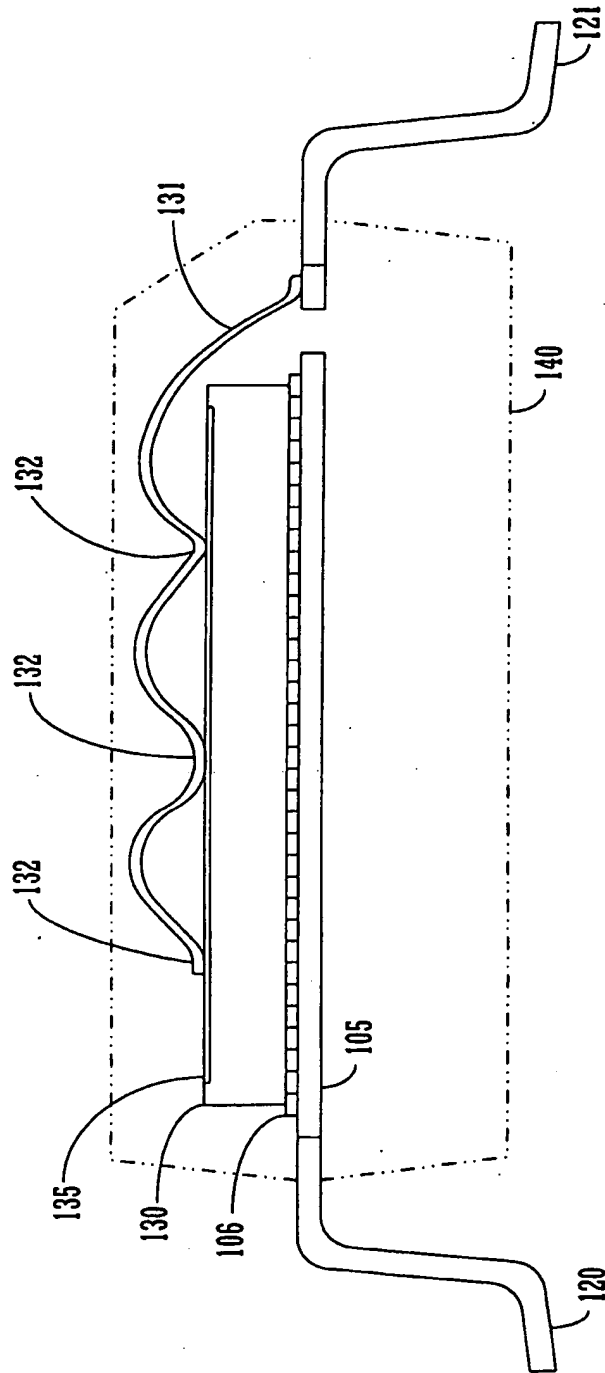
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-- Prior Art --
FIGURE 1

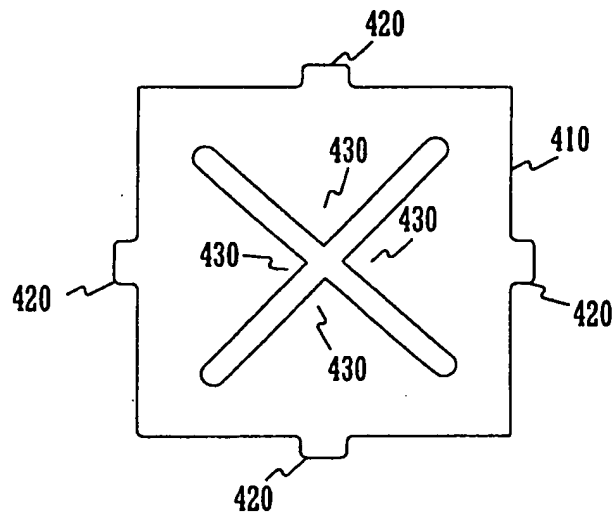
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-- Prior Art --

FIGURE 2

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-- Prior Art --

FIGURE 4

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